APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SECOND SEMESTER M. TECH DEGREE EXAMINATION
Electronics & Communication Engineering
(VLSI and Embedded Systems)
04EC6503—ADVANCED DIGITAL DESIGN

Max. Marks: 60 Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. Illustrate Shannon's expansion theorem
2. Write down the behavioral description of a mod10 synchronous counter.
3. Explain about races in asynchronous sequential circuits.
4. Design a clock divider which converts 60Hz input clock frequency to 1Hz output clock.
5. Describe RTL design steps.
6. Illustrate the significance of critical path delay in determining the clock frequency of a circuit.
7. Draw HLSM for a Laser-Based Distance Measurer.
8. Explain RTL design optimization with operator binding.

PART B

Each question carries 6 marks

9. Design a Mealy FSM to detect the occurrence of sequence 1011 in a serial communication datapath.

OR

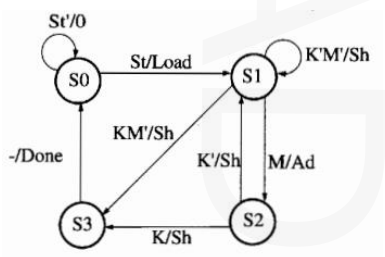
10. Design a clocked synchronous state machine with the state/output table shown in, using D flip-flops. Use two state variables, Q1 Q2, with the state assignment A = 00, B = 01, C = 11, D = 10.

PS	NS		Z
	X=0	X=1	
A	B	D	0
B	C	B	0
C	B	A	1
D	B	C	0

11. Explain in detail about different types of static hazards with example

OR

12. Convert the given state graph to SM chart

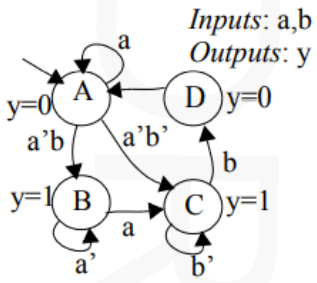


13. Design an 8-bit register with 2 control inputs s1 and s0, 8 data inputs I7...I0, and 8 data outputs Q7...Q0. s1s0=00 means maintain the present value, s1s0=01 means load, and s1s0=10 means clear. s1s0=11 means reverse its bits.

OR

14. Using the five–step process for designing a controller, design a Gray code sequencer with an input gcnt and three outputs, x, y and z. The Gray code sequence that the FSM should output is 000, 010, 011, 001, 101, 111, 110, 100, repeat. The output should change only on a rising clock edge when the input gcnt = 1. Make the initial state 000.

15. Using the process for designing a controller, convert the given FSM to a controller, implementing the controller using a state register and logic gates.



OR

16. A wristwatch display can show one of four items: time, alarm, stopwatch, or date, controlled by two signals S1 and S0 (00 displays the time, 01 the alarm, 10 the date, and 11 the stopwatch). Pressing a button B (which sets B=1) sequences the display to the next item in the order listed above. Create a state diagram for an FSM describing this sequencing behavior, having an input B and two output bits S1 and S0.
17. Using RTL design method create an RTL that outputs the maximum value found within a register file A consisting of 64 32-bit numbers.

OR

18. Design a HLSM for soda machine dispenser. Design datapath to structure and controller to FSM for the same.
19. Design an area optimized 3-tap FIR filter.

OR

20. Design a pipelined adder tree to compute the sum of eight inputs on every clock cycle, where the sum is S = A + B + C + D + E + F + G + H + I. What is the latency and throughput of the adder if the single stage adder has a delay of 4ns?